ABSTRACT

An SMII interface circuit to communicate data synchronous with a clock signal having a rising edge and a falling edge. The interface circuit includes a transmit circuit that is responsive to the clock signal to generate a first transmit serial stream and a second transmit serial stream. A receive circuit, responsive to the clock signal, to generate a receive serial stream from two receive data streams. The receive serial stream having a operating frequency that is about twice the operating frequency of each of the two receive data streams. Transmit and receive ports corresponding to the transmit and receive circuits each include a single pin to communicate the serial transmit data and the receive serial stream.

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